

REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application as amended.

Claims 1-5, 7-9, 26-32, and 34-40 are pending in the present application.

Claims 1-5, 7-9, 26-32, and 34-40 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 6,109,201 ("Petranovic").

In particular, the Examiner has stated in part that

As to claims 1, 26, 35, 39 and 40 Petranovic et al. teach a method for designing a system on a target device utilizing filed programmable gate arrays (FPGA), comprising: identifying a group of components associated with a critical signal in the system (see fig 1a, 1b, col 2 line 15 to col 4 line 3, especially col 3 line 20 to col 4 line 3, and col 5 line 3-21); creating a first copy (fig 4 element 62) and a second copy (see fig 4 element 64) of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state (see fig 3-5, col 5 line 23 to col 6 line 48; especially fig 4 element 62, 64, and 66 col 6 line 20-29, and summary); and configuring the system utilizing a selector circuit on the target device to select an output of one of the first copy and the second copy in response to the critical signal (see fig 3, fig 4, fig 5 col 5 line 41 to col 6 line 68; especially fig 5 element 68 col 5 line 46 to col 6 line 47), and removing the group of components identified such that only the first copy and the second copy of the group of components represent the group of components identified (see fig 2-5 col 5 line 3 to col 8 line 42).

(5/13/2008 Office Action, pp. 2-3)

It is submitted that Petranovic does not render claims 1-5, 7-9, 26-32, and 34-40 unpatentable under 35 U.S.C. §102(b).

Petranovic includes a disclosure of a method and apparatus for transforming the circuits comprising the critical path, thereby increasing the performance of the entire IC. The transformation is performed by segmenting, or blocking, the cells which make up the critical path. Then, each block is transformed, or replaced, with a resynthesized circuit to which both the digital 0 and digital 1 values are provided. The critical path is defined by the fact that the delay

at each block is accumulated because each block has to wait for the output signal of the preceding block to use as its input signal. After the resynthesis of the blocks, none of the blocks need to wait for the output signal of its preceding block because each of the resynthesized blocks has the output for all possible inputs values (0 and 1). Thus, the signal delay at each block is not accumulated; rather, the only accumulated delay is the delay of the multiplexors used to select the correct output. The result is a dramatically reduced critical path delay (see Petranovic Abstract).

Applicants submit that Petranovic does not teach or suggest identifying a group of components associated with a critical signal in the system, creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state, configuring the system to utilize a selector circuit on a target device to select an output of one of the first copy and the second copy in response to the critical signal, and removing the group of components identified such that only the first copy and the second copy of the group of components represent the group of components identified.

The Examiner cites Figure 4, element 62 and Figure 4, element 64 for support that Petranovic discloses creating a first copy and a second copy of a group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state (see 5/13/2008 Office Action, p. 2). Applicants submit that Figure 4 does not illustrate an element 62 and 64. Figure 5, illustrates an element 62 and 64. Block 62, however, is a first block that is driven by a critical input I_i , not a first signal at a first state (see Petranovic column 6, lines 31-32, and Figure 5).

Furthermore, Petranovic discloses representing a group of components identified with more than a first copy of the components driven by a first signal at a first state and a second copy of the components driven by a second signal at a second state. Petranovic discloses a resynthesized circuit 60 that includes three blocks of cells. A first block 62 is provided with a

critical input I_i . A second block 64 is provided a zero as its critical input. A third block 66 is provided a one as its critical input. Figure 5 illustrates that all non-critical path outputs, Z_i , are taken from the first block 62, and critical path outputs are taken from the second block 64 and the third block 66 (see Petranovic column 6, lines 20-43 and Figure 5). Petranovic discloses that the three blocks of cells 62, 64, and 66 used to represent the original block of cells, B_i 54, may be identical to each other and identical to the original block of cells (see Petranovic column 6, lines 22-24 and Figure 4 and 5).

Petranovic specifically states that the first block 62 is the original block where the second block 64 is a first copy of the original block and the third block 66 is a second copy of the original block (see Petranovic column 6, lines 25-29). The first block 62 (original block) is an integral component in the resynthesized circuit 60. The first block 62 is never removed from the resynthesized circuit 60. Clearly, Petranovic does not teach or suggest removing a group of components identified such that only the first copy and the second copy of the group of components represent the group of components identified.

Applicants submit that Petranovic fails to disclose the removal of a group of components identified as being a group of components associated with the critical signal in the system such that only the first copy and the second copy of the group of components represent the group of components identified. Applicants respectfully request that the Examiner clarify where he believes Petranovic discloses the removal of the group of components identified or the removal of any components.

In contrast, claim 1, as amended, states

A method for designing a system on a target device utilizing field programmable gate arrays (FPGAs), comprising:
identifying a group of components associated with a critical signal in the system;
creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state;

configuring the system to utilize a selector circuit on the target device to select an output of one of the first copy and the second copy in response to the critical signal; and removing the group of components identified such that only the first copy and the second copy of the group of components represent the group of components identified.

(Claim 1, as amended) (Emphasis Added).

Claims 31, 35, and 39 include the limitation of having only the first copy and the second copy of the group of components represent the group of components identified. Given that claims 2-5, 7-9, and 37 depend from claim 1, and 36 depend from claim 35, it is likewise submitted that claims 2-5, 7-9, and 36-37 are also patentable under 35 U.S.C. §102(b) over Petranovic.

Applicants submit that Petranovic also does not teach or suggest determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique to resolve illegalities in placement by moving components not associated with the critical signal to allow the first copy and the second copy to be placed at preferred locations.

In the Office Action mailed 5/13/2008, the Examiner states in part that

As to claims 8, 33, and 36 Peranovic et al. teach further comprising determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique to resolve illegalities in placement by moving components not associated with the critical signals to allow the first copy and the second copy to be placed at preferred locations (see fig 4, fig 5 col 5 line 30 to col 6 line 47).

(5/13/2008 Office Action, p. 4) (Emphasis Added).

Applicants submit that Petranovic discloses a resynthesis methodology where a circuit is transformed by segmenting cells which make up a critical path into blocks. Each block is replaced by 3 identical blocks and a multiplexer. The first block receives non-critical inputs. A zero is provided to the second block as a critical input and a one is provide to the third block as a critical input (see Petranovic Abstract and col. 4, lines 24-32). Petranovic, however, does not

teach or suggest how and where the blocks or are placed. Petranovic focuses only on the resynthesis technique but provides no solution as to placement on a device (see Petranovic columns 4-9, and Figures 2-5).

Furthermore, Applicants submit that Petranovic does not provide any disclosure on how to resolve illegalities in placement, nor does Petranovic provide any disclosure regarding an incremental placement technique that moves components not associated with a critical signal to allow the first copy and second copy to be placed at preferred locations. Moreover, the text cited by the Examiner, column 5, line 30 to column 6, line 47, does not make any reference to "placement", "preferred locations", or "moving components". Applicants have requested that the Examiner clarify the relevance of the cited text (10/12/2008 Response, p. 9, and 3/10/2008 Amendment, p. 11), but have not received any clarification as to the why the Examiner believes that the cited text is relevant.

In contrast, claim 26 states

A machine-readable medium having stored thereon sequences of instructions, the sequences of instructions including instructions which, when executed by a processor, causes the processor to perform:

identifying a group of components associated with a critical signal in a system;

creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state;

configuring the system to utilize a selector circuit to select an output of one of the first copy and the second copy in response to the critical signal; and

determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique to resolve illegalities in placement by moving components not associated with the critical signal to allow the first copy and the second copy to be placed at preferred locations.

(Claim 26) (Emphasis Added).

Claims 8 and 36 include similar limitations. Given that claims 27-32, 34, and 38 depend from claim 26, it is likewise submitted that claims 27-32, 34, and 38 are also patentable under 35 U.S.C. §102(b) over Petranovic.

Applicants submit that Petranovic also does not teach or suggest identifying a group of components associated with a critical signal in the system, creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state, wherein identifying the group of components includes determining a transitive fanout of the critical signal within a maximum number of logic levels.

The Office has rejected claims 3 and 28 under 35 U.S.C. §102(b) as being unpatentable over Petranovic. In particular, the Examiner has stated in part that

As to claim 3, and 28 Petranovic et al. teach wherein determining the transitive fanout for the critical signal comprises identifying the transitive fanout within a maximum number of logic levels (see fig 2, fig 4 col 5 line 3 to col 6 line 19, and background).

(5/13/2008 Office Action, p. 3) (Emphasis Added).

Applicants submit that Figure 2 of Petranovic only illustrates a critical path and critical path cells on an integrated circuit chip. Figure 4 of Petranovic only illustrates a critical path as defined by a series of blocks. Column 5, line 3 through column 6 line 19 of Petranovic describes a resynthesis procedure where each of the blocks of cells along a critical path, B₁ to B_n, are replaced by a resynthesis circuit shown in Figure 5 (see Petranovic column 5, lines 41-45). Petranovic clearly does not impose a maximum number of logic levels when identifying a group of components on the critical path to resynthesize. In fact, Applicants submit that Petranovic does not refer to logic levels anywhere in the entire patent. Applicants respectfully request the Examiner to clarify the relevance of the cited text and to specifically point out where he believes Petranovic discloses identifying transitive fanout within a maximum number of logic levels when identifying a group of components associated with a critical signal in a system.

In contrast, claim 3 states

The method of Claim 2, wherein determining the transitive fanout for the critical signal comprises identifying the transitive fanout within a maximum number of logic levels.

(Claim 2) (Emphasis Added).

Claim 28 includes similar limitations.

Applicants submit that Petranovic also does not teach or suggest identifying a group of components associated with a critical signal in the system, creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state, wherein identifying the group of components includes determining a transitive fanout of the critical signal, identifying side inputs to the transitive fanout, and determining whether the side inputs have sufficient slack.

The Examiner has rejected claims 4 and 29 under 35 U.S.C. §102(b) as being unpatentable over Petranovic. In particular, the Examiner has stated in part that

As to claim 4, and 29 Petranovic et al. teach further comprising: identifying side inputs to the transitive fanout (see fig 2-5 col 5 line 14 to col 8 line 48); and determining whether the side inputs have sufficient slack (see fig 2-5 col 5 line 14 to col 8 line 48).

(5/13/2008 Office Action, p. 3) (Emphasis Added).

The Office cites 4 figures and 4 columns of text as support that Petranovic determines whether side inputs have sufficient slack. Applicants submit that the sections of text and figures cited do not discuss or disclose determining whether side inputs to a transitive fanout have sufficient slack. In fact, Applicants submit that no where in Petranovic is the term "transitive fanout" or "slack" even mentioned. Applicants respectfully request the Examiner to clarify the relevance of the cited text.

In contrast, claim 4 states

The method of Claim 2, further comprising:
identifying side inputs to the transitive fanout; and
determining whether the side inputs have sufficient slack.

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(Claim 4) (Emphasis Added).

Claim 29 includes similar limitations.

Furthermore, new claims 37-38, and 40 include the limitation of "identifying components in the transitive fanout as a group of components associated with the critical system if the side inputs have slack greater than an amount of delay introduced by a selector circuit"

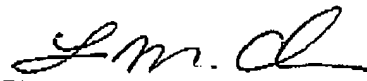
In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-5, 7-9, 26-32, and 34-40 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicant's attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

Dated: September 15, 2008



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